

February 18, 2004

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Aavenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/755,498 01/12/04

Bor-Wen Chan et al.

A METHOD OF FORMING A STACKED CAPACITOR STRUCTURE WITH INCREASED SURFACE AREA FOR A DRAM DEVICE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February ? }, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

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- U.S. Patent 6,025,225 to Forbes et al., "Circuits with a Trench Capacitor Having Micro-Roughened Semiconductor Surfaces and Methods for Forming the Same," discloses a trench cap process with roughened sides.
- U.S. Patent 5,923,989 to Lin et al., "Method of Fabricating Rugged Capacitor of High Density DRAMs," reveals a stacked Cap process with Hemispherical grains (HSG).
- U.S. Patent 5,691,221 to Jun, "Method for Manufacturing Semiconductor Memory Device Having a Stacked Capacitor," discloses a fin capacitor.
- U.S. Patent 5,670,405 to Tseng, "Method of Making a Tooth Shaped Capacitor Using Ion Implantation," discloses a method of manufacturing a capacitor for use in semiconductor memories.
- U.S. Patent 5,801,089 to Kenney, "Method of Forming Stacked Devices," discloses chips having subsurface structures within or adjacent to a horizontal trench in bulk single crystal semiconductors.

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U.S. Patent 6,057,205 to Wu, "Method to Form a Ragged Poly-Si Structure for High Density DRAM Cells," discloses a method for fabricating a capacitor on a semiconductor device.

Sincerely,

Stephen B. Ackerman, Reg. #37761

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